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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/072,872	KANAMORI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8-20,22,24,25 and 27-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20,36 and 37* is/are allowed.

6)☒ Claim(s) *1,3,5,6,8-19,22,24,25,27-35,38 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/21/05 has been entered.

Specification

2. The amended to the specification filed on 3/21/05 is still objected to because the reaction "Fig. 29 is a circuit ... the invention;" on line 9-10 of page 2 of the amendment 3/21/05 is not line-through so the above recitation is not deleted and thus it still causes the new-matter's objection to the specification as discussed in the final office action mailed on 9/22/04. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3, 5, 6, 8-19, 22, 24, 25, 27-35, 38 and 39 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With respect to claim 1, the original disclosure, at the time of filing the application, does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including a fourth transistor for supplying the drive current at the time of signal determination as recited in the claim, i.e., the disclosure does not disclose such third transistor that provides a minute current and also a drive current wherein the third transistor is connected in parallel to the fourth transistor that provides the drive current.

Claims 3, 5, 6 and 8-16 depend on claim 1, so they are rejected under 35 U.S.C. 112, first paragraph, for the same reason as in claim 1.

With respect to claim 17, the original disclosure, at the time of filing the application, does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including a fourth transistor for supplying the drive current at the time of signal determination as recited in the claim, i.e., i.e., the disclosure does not disclose such third transistor that provides a minute current and also a drive current wherein the third transistor is connected in parallel to the fourth transistor that provides the drive current.

Claims 18, 19, 22, 24, 25, 27-35 depend on claim 17, so they are rejected under 35 U.S.C. 112, first paragraph, for the same reason as in claim 17.

With respect to claims 38 and 39, the original disclosure, at the time of filing the application, does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including an eighth transistor as recited in the claim, wherein the third

transistor doubles as a transistor for supplying a drive current at the time of signal determination, i.e., there is no such third transistor for providing a minute current and also for providing a drive current at the time of signal determination connected with the eighth transistor as recited in the claims.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 3, 5, 6, 8-16, 17-19, 22, 24, 25, 27-35, 38 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, this claim is indefinite because the claim is misdescriptive since there is no such differential amplifier circuit having a third transistor for keeping a minute current to flow and also supplying a drive current at the time of signal determination, and a fourth transistor for supplying the drive current at the time of signal determination wherein the third transistor is connected in parallel with the fourth transistor. Note that, in Figures 8-9 and 13-17, the third transistor (3) only for keeping the minute current to flow, and the fourth transistor (30) is for supplying the drive current at the time of signal determination; and that the third transistor (3) in Figures 8-9 and 13-17 does not also supply the drive current at the time of signal determination. Note that, the disclosure only discloses in Figure 11A that transistor 30' for keeping a minute current to flow (when CK is Low) and also for supplying a drive current at the time of signal determination (when CK is Hi), but Figure 11A does not show a fourth transistor for supplying the drive current, wherein the fourth transistor is connected in parallel with the third transistor.

Claims 3, 5, 6 and 8-16 are indefinite because they include the indefiniteness of claim 1.

Also in claim 5, the recitation "the control electrode of said third transistor is supplied with a first control signal for supplying the minute current during the operation of said differential amplifier and a second control signal for supplying the drive current" is misdescriptive as discussed above. Note that the third transistor (3, Figures 8-9 and 13-17) is supplied with only one control signal PDX for supplying the minute current, and there is no second control signal for supplying the drive current. Also note that Figure 11A shows the third transistor (30') is supplied with a first control signal (signal at node M in Figure 11B) for supplying the minute current to flow (when CK is Low) and a second control signal (signal at node H in Figure 11B) for supplying the drive current at the time of signal determination (when CK is Hi), but Figure 11A does not show a fourth transistor for supplying the drive current, wherein the fourth transistor is connected in parallel with the third transistor.

Also in claim 8, this claim is also indefinite for the similar reason as discussed in claims 1 and 5 above. Note that the third transistor (3, Figures 8-9 and 13-17) is only supplied with a control signal PDX for supplying the minute current, but does not supply the drive current. Also note that Figure 11A shows the third transistor (30') is supplied with a control signal (CCS) for supplying the drive current at the time of signal determination (when clock CK is Hi) while causing the minute current to flow at other than the time of signal determination (i.e., when clock CK is Low), but Figure 11A does not show a fourth transistor for supplying the drive current, wherein the fourth transistor is connected in parallel with the third transistor.

Claim 17 is indefinite for the similar reasons as discussed in claim 1 above, i.e., there is no such differential amplifier circuit having a third transistor for keeping a minute current to

flow and also supplying a drive current at the time of signal determination, and a fourth transistor for supplying the drive current at the time of signal determination wherein the third transistor is connected in parallel with the fourth transistor. Note that, in Figures 8-9 and 13-17, the third transistor (3) only for keeping the minute current to flow, and the fourth transistor (30) is for supplying the drive current at the time of signal determination; and that the third transistor (3) in Figures 8-9 and 13-17 does not also supply the drive current at the time of signal determination. Note that, the disclosure only discloses in Figure 11A that transistor 30' for keeping a minute current to flow (when CK is Low) and also for supplying a drive current at the time of signal determination (when CK is Hi), but Figure 11A does not show a fourth transistor for supplying the drive current, wherein the fourth transistor is connected in parallel with the third transistor.

Claims 18, 19, 22, 24, 25 and 27-35 are indefinite because they include the indefiniteness of claim 17.

Also, claims 24 and 27 are also indefinite for the similar reasons as discussed above with regard to claims 5 and 8, respectively.

With respect to claim 38, this claim is indefinite because there is no such differential amplifier circuit having a third transistor for keeping a minute current to flow and also supplying a drive current at the time of signal determination, and an eighth transistor with the connections as recited in the claim. Note that, in Figure 17, the third transistor (3) only for keeping the minute current to flow, and is not supplying the drive current at the time of signal determination. Note that, the disclosure only discloses in Figure 11A that transistor 30' for keeping a minute current to flow (when CK is Low) and also for supplying a drive current at the time of signal

determination (when CK is Hi), but Figure 11A does not show an eighth transistor with the connections as recited in the claim.

Claim 39 is indefinite for the same reasons as discussed in claim 38 above.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 6, 9, 10 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Branson et al. (USP 5,508,664).

Insofar as understood in claim 1, Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10), which includes: a latch unit (12, 14, 16, 18) and a differential input portion (22, 20) comprising a first transistor (22) and a second transistor (20); a third transistor (26) for supplying the minute current (small current that transistor 26 sinks, see lines 5-6, Col. 3); and a fourth transistor 24) for supplying a drive current at the time of signal determination (i.e., when LE is Hi); wherein the third transistor (26) is connected in parallel with the fourth transistor (24). Note that, due to the indefiniteness as discussed above, the connection of the third and fourth transistor in the differential sense amplifier in Figure 1 of Branson et al. is similar as applicant's invention (e.g., Figure 8 of applicant's invention), so if the third transistor (3) of applicant's invention also provides the drive current at the time of signal determination, then the third transistor (26) of Branson also provides the drive current at the time of signal determination.

Insofar as understood in claim 3, the third transistor (26) turns off the minute current (small current that transistor 26 sinks) flowing through the first (22) and second (20) transistors upon deactivation (power off) of the differential sense amplifier circuit (10). This is because upon deactivation (power off) of the differential sense amplifier circuit (10), n-channel transistor 26 will be turned off since the gate of this transistor receives no power supply (power off). Thus, transistor 26 turns off the small current flowing through transistors 22 and 20.

Insofar as understood in claim 6, Col. 2, lines 35-40, of the Branson et al. reference discloses that a gate width of the third transistor (26) is smaller than a gate width of the fourth transistor (24).

Insofar as understood in claim 9, Figure 1 of the Branson et al. reference shows that the latch unit (12, 14, 16, 18) includes a first inverter (14, 18) inserted between the second electrode of the first transistor (22) and a second power supply (Vdd); and a second inverter (12, 16) inserted between the second electrode of the second transistor (20) and the second power supply line (Vdd), the first and second inverters being cross-coupled to each other.

Insofar as understood in claim 10, Figure 1 of the Branson et al. reference shows that the differential sense amplifier circuit (10) is configured of MOS transistors; transistors (14 and 12) of the first (14, 18) and second (12, 16) inverters which are connected to the second power line (VDD) are each connected in parallel with an additional transistor, respectively (transistor 14 is connected in parallel with transistor 36, and transistor 12 is connected in parallel with transistor 34); and the second electrode of each of the first (22) and second (20) transistors is held at a predetermined level at other than the time of signal determination during the operation of the differential sense amplifier (e.g., when LE is at low level, p-channel transistors 36 and 34 are

turned on because the gates of these transistors receive a logic low to pull the outputs of the first and second inverters to logic high (power supply Vdd level); n-channel transistors 18 and 16 receive the logic high (power supply Vdd level) at their gates so that n-channel transistors 18 and 16 are turned on and the second electrode of each of the first (22) and the second (20) transistors also having the power supply Vdd level. Therefore, the second electrode of each of the first and second transistors is held at a predetermined level (logic high) when LE is at low level during operation of the differential sense amplifier.

Insofar as understood in claim 16, the differential sense amplifier (10) in Figure 1 of the Branson et al. reference is a differential sense amplifier circuit (10) of a strong arm latch type (the differential sense amplifier in Figure 1 of the Branson et al. reference has a latch unit portion, and has the same structure as that of the applicant's invention).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (each of Figures 1-7) in view of Branson et al. (UPS 5,508,644).

Insofar as understood in claims 11-15,Each of Figures 1-7 of the applicant's admitted prior art shows a differential sense amplifier circuit which includes: a latch unit (111, 112, 121, 122); a differential input portion (101, 122) and a transistor (130) for supplying a drive current except for a minute current is kept to flow through the differential input portion. However,

Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10) which includes a small transistor (26) for keeping a small current to flow through the input transistors 20 and 22 for the purpose of sensing a small voltage differential across the input terminals and suitable for use in high speed applications (see line 62 of Col.1 to line 10 of Col. 2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential amplifier in each of Figures 1-7 of the applicant's admitted prior art with the small transistor, as taught in Figure 1 of the Branson et al. reference, for the purpose of sensing a small voltage differential across the input terminals of the differential amplifiers and suitable for use in high speed applications. Note that, due to the indefiniteness as discussed above, the connection of the third and fourth transistor in the differential sense amplifier in Figure 1 of Branson et al. is similar as applicant's invention (e.g., Figure 8 of applicant's invention), so if the third transistor (3) of applicant's invention also provides the drive current at the time of signal determination, then the third transistor (26) of Branson also provides the drive current at the time of signal determination. Also note that, in each of these combinations (e.g., each of Figures 1-7 of applicant's admitted prior art and the Branson et al. reference), a minute current (small current that the small transistor 26 sinks from transistors 101 and 102 in each of Figures 1-7 of the applicant's admitted prior art) is kept to flow through the differential input portions. Also, in each of these combinations, the differential input portion (101-102) comprising a first transistor (101) and a second transistor (102); a fourth transistor (130 in each of Figures 1-7 of applicant's admitted prior art), and a third transistor (26 as taught Figure 1 of the Branson et al. reference) of the differential amplifier includes:

In claim 11, the combination of Figure 2 of applicant's admitted prior art and the Branson et al. reference as discussed above shows a fifth transistor (140) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102) for shorting the second electrodes of the first and second transistors in accordance with a second control signal (CK).

In claim 12, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference as discussed above shows a sixth transistor (150) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102), wherein the sixth transistor having a control electrode (gate) supplied with a predetermined voltage (AVD).

In claim 13, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference as discussed above meets the limitation "wherein said differential input signal is at CML level" (see the description of Figure 3 of applicant's admitted prior art on lines 5-9, page 10, of the instant specification).

In claim 14, the combination of Figure 4 of applicant's admitted prior art and the Branson et al. reference as discussed above shows a seventh transistor (160) inserted between two nodes (q, qx) for retrieving a differential output signal (q, qx), the seventh transistor (160) shorting the two nodes in accordance with a third control signal (CK).

In claim 15, the combination of Figure 7 of applicant's admitted prior art and the Branson et al. reference as discussed above shows an eighth transistor (170) connected between the second power supply (AVD) and the common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first (101) and second (102) transistors are

connected, a control electrode (gate) of the eighth transistor (170) being supplied with a fourth control signal (CK).

11. Claims 17, 18, 22, 25 and 28-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (each of Figures 1-7) in view of Branson et al. (UPS 5,508,644) and Oklobdzija et al. (USP 6,232,810).

Insofar as understood in claim 17, each of the above combinations (each of Figures 1-7 of applicant's admitted prior art and the Branson et al. reference as discussed in section 5 above) discloses a semiconductor device having a differential amplifier circuit (each of the above combinations), and a clock source (inherently, i.e., whichever source that is used to generate the clock signal CK in each of Figures 1-7 of applicant's admitted prior art) generating a clock (CK) and supplying the generated clock (CK) to the differential amplifier circuit, wherein the differential amplifier circuit includes a latch unit (111, 112, 121, 122), a differential input portion (101, 102) comprising first and second transistors, a third transistor (26 in Figure 1 of Branson et al. as discussed in the combination and a fourth transistor (130), see the combination of each of Figures 1-7 of applicant's admitted prior art and the Branson et al. reference as discussed in section 10 above for detail discussion. While each of the above combinations fails to disclose the semiconductor device includes a latch circuit latching an output signal of the differential amplifier circuit, the Oklobdzija et al. reference discloses that an SR latch circuit connected to the output of the differential sense amplifier to latch the output of the differential sense amplifier for the well-known purpose of making a D flip-flop circuit (see Figures 1 and 3, lines 13-15 of Col. 1, and lines 11-12 of Oklobdzija et al.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential

sense amplifier in each of the above combinations (each of Figures 1-7 of the applicant's admitted prior art and the Branson et al. reference) with an SR latch circuit connected at the output of the differential sense amplifier for the purpose of making a D flip-flop circuit for use in digital systems, such as processors, digital signal processors and memories. Thus, each of these combinations meets all the limitations of claim 17.

Insofar as understood in claim 18, each of the above combinations (each of the Figures 1-7 of applicant's admitted prior art and the Branson et al. reference, and the Oklobdzija et al. reference) meets all the limitations of this claim, e.g., the semiconductor integrated circuit device is a receiving circuit (any circuitry that receives an input signal can be construed as a receiving circuit) of a signal transmission system (e.g., digital systems such as processors or memories that the differential D Flip-flop is used in), the signal transmission system including a transmission circuit (inherently, e.g., whichever circuit that is used to generate the differential signal d and dx for inputting to the differential sense amplifier) outputting the differential signal, a signal transmission path (the wires connected between the output of the circuit that is used to generated differential signal d and dx to the input of the differential sense amplifier), and the receiving circuit receiving the differential signal through the signal transmission path (the wires).

Insofar as understood in claim 22, in each of these combinations, the third transistor (26, Figure 1 of Branson et al.) turns off the minute current (small current that transistor 26 sinks) flowing through the first (101) and second (102) transistors upon deactivation (power off) of the differential sense amplifier circuit. This it because upon deactivation (power off) of the integrated circuit device, n-channel transistor 26 will be turned off since the gate of this transistor

receives no power supply (power off) and thus transistor 26 turns off the small current flowing through the first and second transistors.

Insofar as understood in claim 25, each of the combinations (as discussed above with regard to claim 17) meets the limitation that a gate width of the third transistor (26) is smaller than a gate width of the fourth transistor (130).

Insofar as understood in claim 28, each of the combinations (as discussed above with regard to claim 17) shows that the latch unit includes a first inverter (111-112) inserted between the second electrode of the first transistor (101) and a second power supply (AVD); and a second inverter (121-122) inserted between the second electrode of the second transistor (102) and the second power supply line (AVD), the first and second inverters being cross-coupled to each other.

Insofar as understood in claim 29, each of the combinations (as discussed above with regard to claim 17) shows that the differential sense amplifier circuit is configured of MOS transistors; transistors (111 and 121) of the first (111, 112) and second (121, 122) inverters which are connected to the second power line (AVD) are each connected in parallel with an additional transistor, respectively (transistor 111 is connected in parallel with transistor 110, and transistor 121 is connected in parallel with transistor 120); and the second electrode of each of the first (101) and second (102) transistors is held at a predetermined level at other than the time of signal determination during the operation of the differential sense amplifier (e.g., when signal CK is at low level, p-channel transistors 110 and 120 are turned on because the gates of these transistors receive the low level so that both nodes q and qx have the same potential as the supply potential AVD, which turns on n-channels transistors 112 and 122 so the second electrode of

each of the first (101) and the second (102) also having the supply potential AVD. Therefore, the second electrode of each of the first and second transistors is held at a predetermined level (supply voltage AVD) when signal CK is at low level during operation of the differential sense amplifier).

Insofar as understood in claim 30, the combination of Figure 2 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows a fifth transistor (140) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102) for shorting the second electrodes of the first and second transistors in accordance with a second control signal (CK). Note that, the Examiner treats this claim as if it depends on claim 21.

Insofar as understood in claim 31, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows a sixth transistor (150) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102) having a control electrode (gate) supplied with a predetermined voltage (AVD). Note that, the Examiner treats this claim as if it depends on claim 21.

Insofar as understood in claim 32, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, meets the limitation "wherein said differential input signal is at CML level" (see the description of Figure 3 of applicant's admitted prior art on lines 5-9, page 10, of the instant specification).

Insofar as understood in claim 33, the combination of Figure 4 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above,

shows a seventh transistor (160) inserted between two nodes (q, qx) for retrieving a differential output signal (q, qx), the seventh transistor (160) shorting the two nodes in accordance with a third control signal (CK).

Insofar as understood in claim 34, the combination of Figure 7 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows an eighth transistor (170) connected between a second power supply (AVD) and the common node (the node connecting transistors 101 and 102 together) to which the first electrodes of the first (101) and second (102) transistors are connected, a control electrode (gate) of the eighth transistor (170) being supplied with a fourth control signal (CK). Note that, the Examiner treats this claim as if it depends on claim 21.

Insofar as understood in claim 35, in each of the combinations as discussed above with regard to claim 17, the differential sense amplifier is a differential sense amplifier circuit of a strong arm latch type.

Allowable Subject Matter

12. Claim 20, 36 and 37 are presently allowed.

Response to Arguments

13. Applicant's arguments filed on 3/21/05 have been fully considered but they are not persuasive.

With respect to the rejections under 35 U.S.C. 112, 1st paragraph, Applicant argues that the third transistor corresponding to a transistor 3 and the fourth transistor corresponding to transistor 30, and applicant submits that the specification (lines 26-30, page 14, "specifically, the transistor 3 is configured as a small transistor having a gate width about one thirtieth the gate

width of the transistor 30. Therefore, a minute current flows constantly in the differential input transistor 1 and 2"; and lines 8-12, page 15, "for signal determination, when clock CK changes from low level "L" to high level "H", the transistor 30 turns on and a current path is formed from the high potential AVD to the low potential power line AVS (ground GND) and the drive current flows") is sufficiently supported the claims limitations. However, these arguments are not persuasive because the third transistor (3, Figures 8-9 and 13-17) only for keeping the minute current to flow, and the fourth transistor (30) is for supplying the drive current at the time of signal determination; and that the third transistor (3) in Figures 8-9 and 13-17 does not also supply the drive current at the time of signal determination, i.e., in Figures 8-9 and 13-17, the third transistor 3 only provides one current (minute current) and does not provide two currents (one for minute current, and another one for the drive current at the time of signal determination). Note that, the disclosure only discloses in Figure 11A that transistor 30' for providing a minute current to flow (when CK is Low) and also for providing drive current at the time of signal determination (when CK is Hi), Figure 11A does not show a fourth transistor for supplying the drive current, wherein the fourth transistor is connected in parallel with the third transistor.

Conclusion

14. Because the scope of claims 5, 8, 19, 24, 27, 38 and 39 cannot be determined due to the indefiniteness as discussed above and the original specification are not also disclosed/supported these claims, no prior art can be applied to these claims at this time. Note that this is not an indication of allowability.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

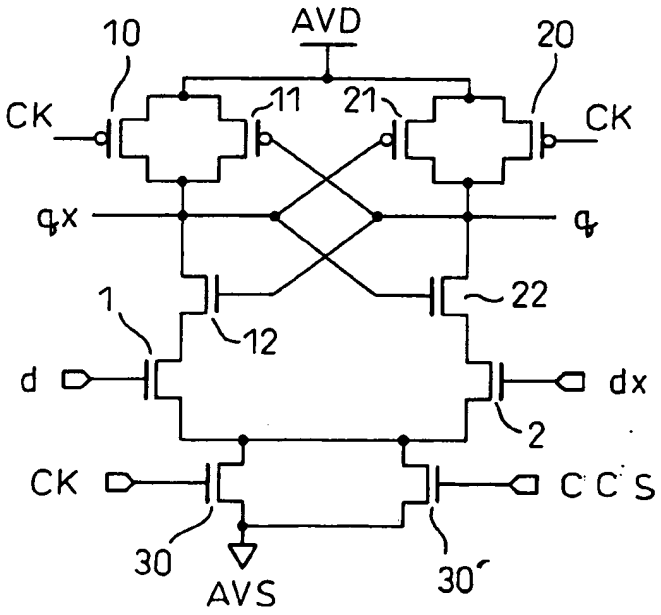
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 26, 2005

LONG NGUYEN
PRIMARY EXAMINER

Not approved!
Do not Enter!
4/26/05 LW

Fig.26



Not approved!
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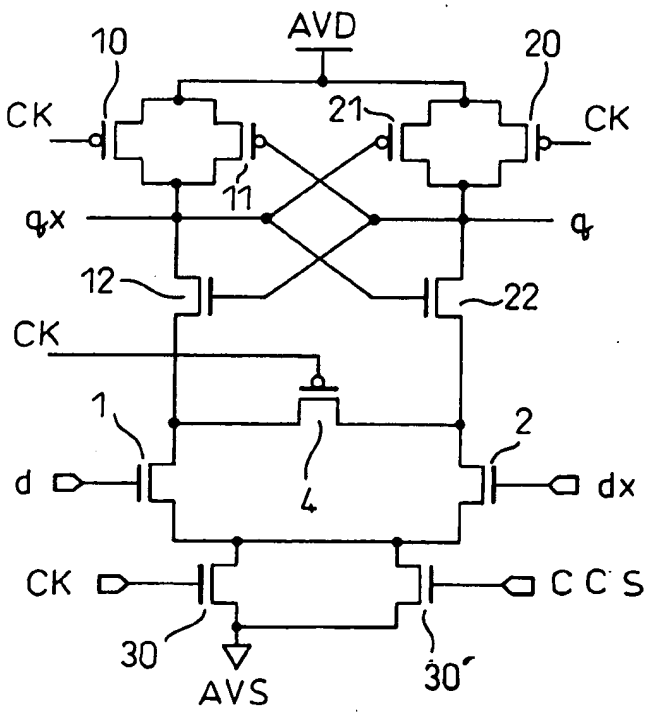
4/26/05 LN

Fig. 27



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4/26/05 LW

Fig.28

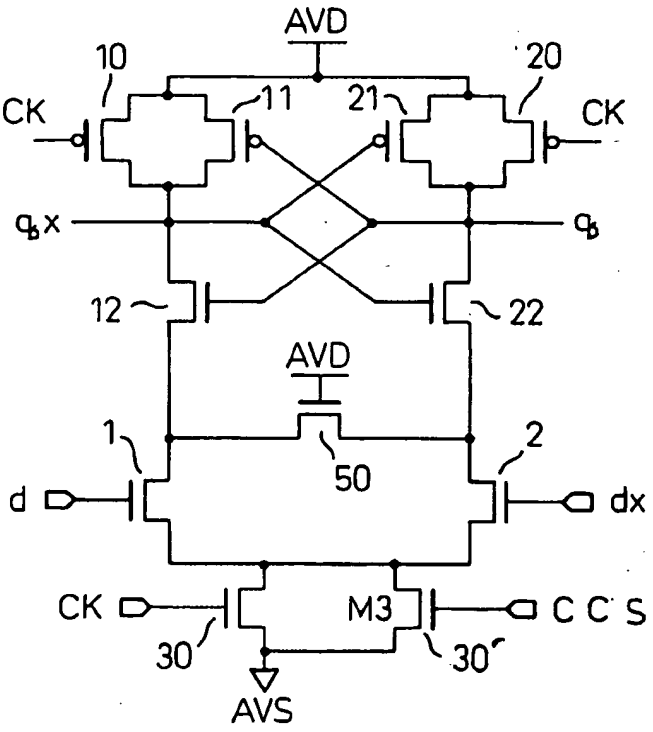

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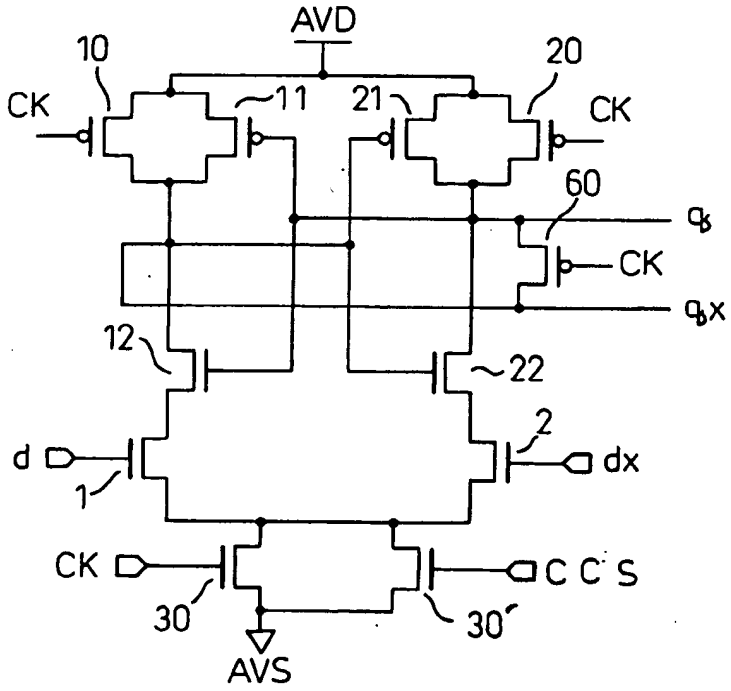
Fig.29



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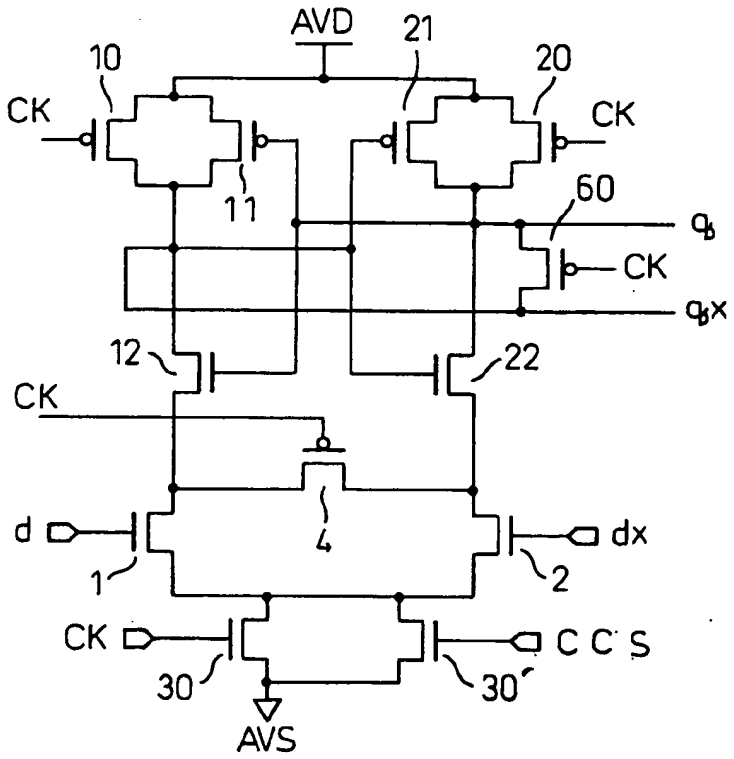
4/26/05 LW

Fig.30



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4/26/05 LW

Fig.31

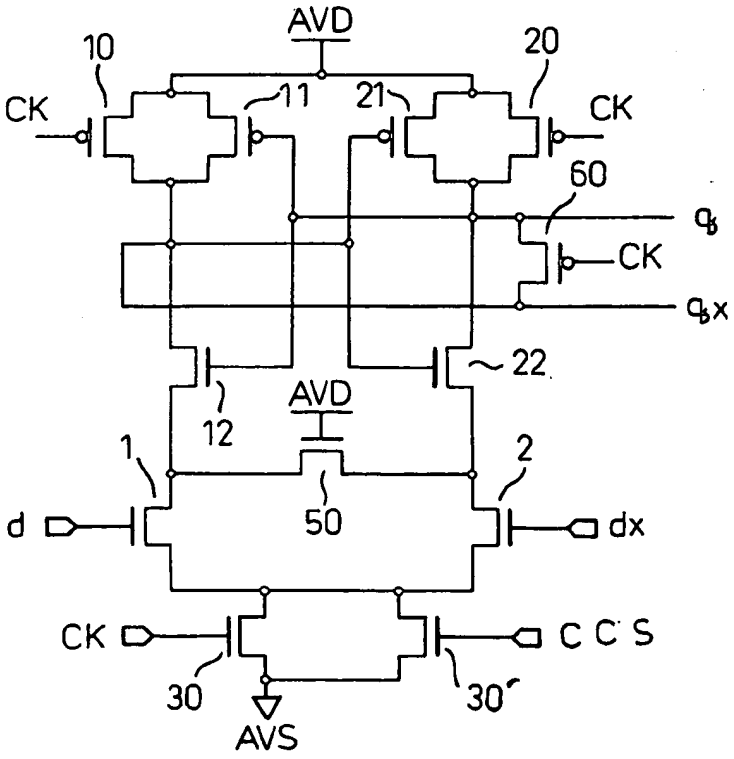

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Fig.32